Breakdown of High-Performance Monolayer MoS_2 Transistors

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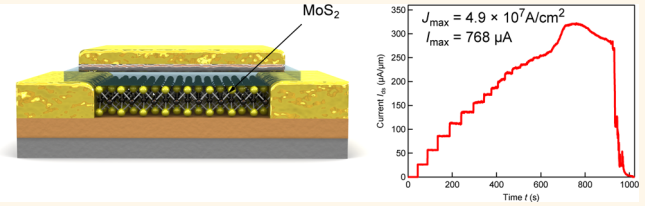
ABSTRACT



Two-dimensional (2D) materials such as monolayer molybdenum disulfide (MoS_2) are extremely interesting for integration in nanoelectronic devices where they represent the ultimate limit of miniaturization in the vertical direction. Thanks to the presence of a band gap and subnanometer thickness, monolayer MoS_2 can be used for the fabrication of transistors exhibiting extremely high on/off ratios and very low power dissipation. Here, we report on the development of 2D MoS_2 transistors with improved performance due to enhanced electrostatic control. Our devices show currents in the 100 μA/μm range and transconductance exceeding 20 μS/μm as well as current saturation. We also record electrical breakdown of our devices and find that MoS_2 can support very high current densities, exceeding the current-carrying capacity of copper by a factor of 50. Our results push the performance limit of MoS_2 and open the way to their use in low-power and low-cost analog and radio frequency circuits.

KEYWORDS: two-dimensional materials · dichalcogenides · MoS_2 · nanoelectronics · breakdown · transistors

Due to their atomic-scale thickness, two-dimensional materials such as graphene and molybdenum disulfide (MoS_2) represent the ultimate limit of material scaling in the vertical dimension. Their planar geometry makes them interesting for incorporation into nanoelectronic devices where they could offer significant power savings due to reduced short channel effects. While graphene has received widespread attention due to its massless charge carriers,[1,2] the lack of an intrinsic band gap limits its applications in electronics to radio frequency (RF) and high-speed analog electronics. Monolayer MoS_2[3] on the other hand is a two-dimensional semiconductor with a direct band gap of 1.8 eV.[4] Silicon-level mobility and high current on/off ratio have recently been demonstrated[5] as well as its ability to amplify signals[6] and perform logic[7] operations in integrated circuits. Its high stiffness and breaking strength[8] also make it interesting for applications in flexible electronics, while the broken inversion symmetry in MoS_2 could be exploited for valleytronics.[9,10]

MoS_2 is a prototypical semiconductor from the transition metal dichalcogenide (TMD) family of materials with the common formula MX_2, where M stands for a transition metal (M = Mo, W, Nb, Ta, Ti, Re) and X for Se, S, or Te. TMD crystals are formed by vertical stacking of layers, 6.5 Å thick. Layers are weakly bonded to each other by van der Waals forces which allows easy cleavage using either the micromechanical cleavage technique[11,12] commonly used for the production of graphene or liquid phase exfoliation.[13] Large-area MoS_2 can also be grown using CVD-like growth techniques.[14,15]

Metal and chalcogenide atoms are strongly bound within the layers, resulting in high mechanical strength, 30 times higher than steel in the case of MoS_2[8] and stability up to 1100 °C in inert atmosphere. MoS_2 is a semiconductor with a band gap that can be tuned by reducing the number of layers: bulk MoS_2 is semiconducting with an indirect band gap of 1.2 eV,[16] while single-layer MoS_2 is a direct gap semiconductor[4,17−19] with a band gap of 1.8 eV[4] due to quantum confinement.[19] The presence of a band gap in single-layer MoS_2 allowed the fabrication of transistors[5] and circuits[7] based on this two-dimensional semiconductor. These transistors showed high mobility (typically 200 $cm^2/V\cdot s$, reaching as high as 780 $cm^2/V\cdot s$) and high current on/off ratios (>10^8). The maximal measured on-current in these devices was 10 μA (2.5 μA/μm) for a drain bias V_{ds} = 500 mV, while the highest transconductance, defined as $g_m = dI_{ds}/dV_{tg}$ observed at V_{ds} = 500 mV was ~4 μS (1 μS/μm). Although these characteristics were extremely promising for applications in low-power digital electronics, several improvements could still be

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Received for review August 18, 2012 and accepted October 2, 2012.

Published online October 05, 2012
10.1021/nn303772b

desirable from the point of view of device performance. For example, the lack of observed saturation together with the relatively low transconductance value would imply low transistor gain,[20,21] an important number for applications in analog electronics and power amplification. In the case of graphene, drain current saturation is very difficult to achieve, with devices in general showing weak saturation[22,23] or no saturation at all.[24]

Furthermore, it is unclear at this point what would be the performance limits and maximal on-current that two-dimensional (2D) MoS_2 field-effect transistors (FET) could support. They have so far been explored only using theoretical calculations in the ballistic regime.[25,26] Here we report a single-layer transistor with enhanced performance due to reduced access resistance and improved electrostatic control due to full-channel gating. Our transistors show a factor of 30 improvement in transconductance, 2 orders of magnitude improvement in the on-current (I_{on} = 600 μA or 250 μA/μm) during normal operation, the first observation of drain current saturation in monolayer MoS_2 transistors, and the highest mobility reported so far for monolayer MoS_2. The high on-current in our devices also allows us to measure the breakdown current density in MoS_2 which is close to 5 $\times$ 10^7 A/cm^2 and 50 times higher than in copper. Our results demonstrate that monolayer MoS_2 could be used in analog circuit applications where it could provide power gain and support large current densities.

RESULTS AND DISCUSSION

Monolayer flakes of MoS_2 were prepared by mechanical cleavage and scotch-tape exfoliation techniques.[12,27] Commercially available bulk crystals of MoS_2 (SPI Supplies Brand Moly Disulfide)[28] served as the material source. The material was deposited on a degenerately doped silicon substrate covered with 270 nm of dry SiO_2 (Figure 1a).[29] Monolayer flakes were detected and distinguished from thicker layers by measuring their optical contrast with respect to the substrate. We have previously established the correlation between contrast and thickness as measured by atomic force microscopy.[29]

Electrical contacts were fabricated applying electron-beam lithography followed by the deposition of 90 nm Au. After acetone lift-off, the devices were annealed for 2 h in inert Ar atmosphere at 200 °C to improve contact resistance and clean the MoS_2 surface before top-gate oxide deposition by atomic layer deposition (ALD). A 30 nm thick layer of HfO_2 serving as the gate dielectric and mobility booster[5,30] is grown on top of MoS_2. A Cr/Au top-gate of 10/50 nm thickness was then fabricated using another electron-beam lithography step (Figure 1b). The substrates were cleaved and glued to a chip carrier. Final interconnects

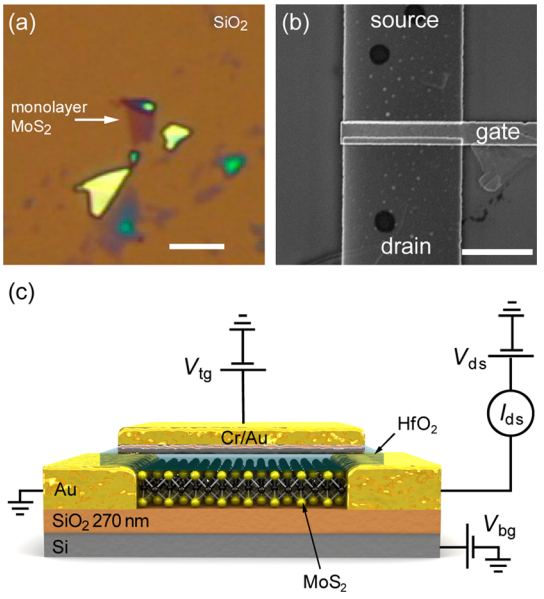

Figure 1. MoS_2 FET device architecture. (a) Optical image of monolayer MoS_2 (6.5 Å thick) exfoliated on a silicon substrate covered with a 270 nm thick SiO_2 layer. Scale bar is 5 μm. (b) SEM image of the final device with a HfO_2 gate dielectric and a local top-gate fabricated on top of the flake shown in a. Au leads of the shown device are separated by 500 nm, and the Cr/Au top-gate is 750 nm long and covers the entire channel between source and drain contact. Scale bar is 2 μm. (c) Three-dimensional representation of the monolayer MoS_2 FET architecture utilized in this study. The Si substrate serves as the back-gate. One of the 90 nm thick Au contacts is grounded, while the other side serves as the drain. The Cr/Au top-gate 10/50 nm thick is separated from the MoS_2 flake by a 30 nm thick HfO_2 layer.

were wire-bonded. Electrical characterization of all devices was performed at room temperature in ambient conditions (air) using an Agilent E5270B parameter analyzer. The cross section of the device is presented in Figure 1c.

This monolayer MoS_2 FET was first characterized by applying a fixed low drain voltage V_{ds} while sweeping the back-gate voltage V_{bg}. In Figure 2a, the corresponding measurement at V_{ds} = 20 mV is depicted. We use the expression for the low-field field-effect mobility $\mu = [dI_{ds}/dV_{bg}] \times [L/WC_iV_{ds}]$, where channel length is L_{ch} = 500 nm, channel width W = 2 μm, and back-gate capacitance $C_i = \varepsilon_0\varepsilon_r/d$ = 1.3 $\times$ 10^{-4} F/m^2 (ε_r = 3.9, d = 270 nm). With this, a field-effect mobility of μ = 1090 cm^2/V·s at a drain voltage of V_{ds} = 20 mV can be estimated. This value is the highest mobility presented to date in MoS_2 FETs and represents a lower limit of the mobility in the 6.5 Å thick semiconducting MoS_2 monolayer since contact resistance is not being accounted for. Errors in the estimate of capacitive coupling could be a further source of experimental uncertainty. A possible cause for the significant increase in mobility could be the fact that in a shorter channel the charge-trap density of the SiO_2 surface right below the 6.5 Å thick charge carrier channel is reduced. Access resistance could also be reduced in

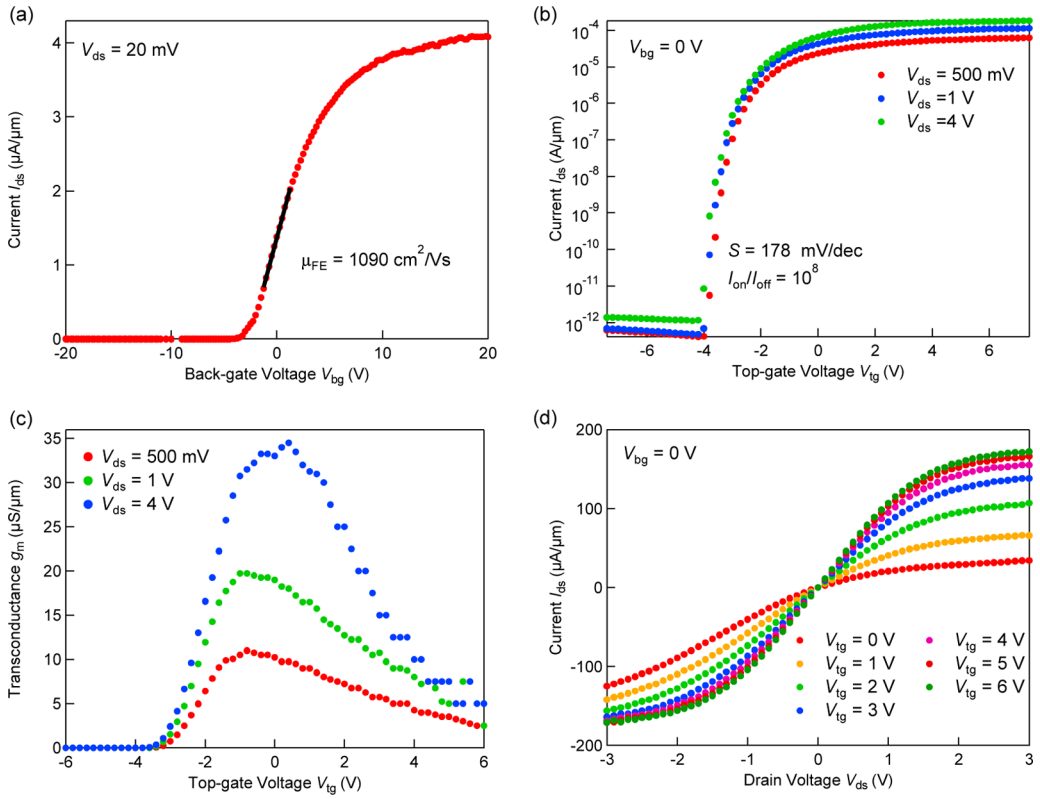

Figure 2. Characterization of a monolayer MoS_2 FET transistor. (a) Room-temperature back-gate transfer characteristic for the MoS_2 FET depicted in Figure 1a,b under the applied drain voltage V_{ds} = 20 mV. We estimate an effective field-effect mobility μ_{fe} = 1090 cm^2/V·s. (b) $I_{ds}-V_{tg}$ curve recorded for three different drain voltages: V_{ds} = 500 mV, 1 V, and 4 V. The I_{on}/I_{off} ratio exceeds 10^8. The subthreshold swing S at V_{ds} = 500 mV is 178 mV/dec. (c) Transconductance $g_m = dI_{ds}/dV_{tg}$ derived from $I_{ds}-V_{tg}$ characteristics shown in b. The peak transconductance for V_{ds} = 4 V is $g_{m,max}$ = 34 μS/μm and is the highest value of transconductance reported for MoS_2 transistors to date. (d) $I_{ds}-V_{ds}$ characteristics measured for different top-gate voltages V_{tg} for drain voltages V_{ds} reaching 3 V. In this device, the on-current is I_{on} = 344 μA (172 μA/μm) for V_{tg} = 6 V and V_{ds} = 3 V, corresponding to a current density of $J = 2.5 \times 10^7$ A/cm^2. This value is 25 times larger than the breakdown current density of copper. At typical bias voltages with V_{ds} exceeding ~2 V, the drain−source $g_{ds} = dI_{ds}/dV_{ds}$ close to 0 (g_{ds} < 2 μS/μm) at V_{ds} = 3 V. At low bias voltages, the curves are linear, indicating that the contacts are ohmic.

this case due to full-channel gating. This motivates further studies on even shorter channel lengths (L_{ch} < 500 nm). In Figure 2b the $I_{ds}-V_{tg}$ characteristics for varying V_{ds} is depicted. The I_{on}/I_{off} ratio for an applied drain voltage of V_{ds} = 4 V and the ±6 V variation of top-gate voltage V_{tg} is on the order of 10^8. This I_{on}/I_{off} ratio exceeds the value of 10^4-10^7 considered necessary for applications in CMOS-like digital circuits.[21,31] At V_{ds} = 500 mV, a subthreshold slope, defined as $S = (d(\log I_{ds})/dV_{tg})^{-1}$, of S = 178 mV/dec can be extracted. In earlier studies, a lower value for the subthreshold slope has been reported.[5] Possible causes for a shallower subthreshold swing in this case could be partial electrostatic shielding of the top-gate by source and drain contacts and a higher trap charge density in either the MoS_2/SiO_2 or MoS_2/HfO_2 interface.

The electrical conductivity of the monolayer MoS_2 can be controlled in a wide range using a top-gate because of the presence of a band gap and large degree of electrostatic control due to its atomic-scale thickness.[25] From the top-gating ($I_{ds}-V_{tg}$ characteristics ($I_{ds}-V_{tg}$) shown in Figure 2b, the transconductance $g_m = dI_{ds}/dV_{tg}$ can be derived. In Figure 2c, we plot the 2D MoS_2 device transconductance for three different drain voltages: V_{ds} = 500 mV, 1 V, and 4 V. The maximal derived transconductance $g_{m,\ max}$ (V_{ds} = 4 V) = 34 μS/μm and is the highest value of transconductance reported for MoS_2 transistors to date. The transconductance at V_{ds} = 1 V is ~20 μS/μm.

Subsequently, the drain−source bias ($I_{ds}-V_{ds}$) characteristic is probed and reported in Figure 2d. For these measurements, the back-gate voltage V_{bg} is kept at 0 V. At relatively low drain voltages exceeding V_{ds} of 1 V, the current-carrying capacity of the MoS_2 charge-carrying channel exhibits saturation, making this the first observation of drain current saturation in monolayer MoS_2 FETs. The drain−source conductance $g_{ds} = dI_{ds}/dV_{ds}$ is close to 0 (g_{ds} < 2 μS/μm) in this region of operation. In this regime, the transistor can operate as a voltage-regulated current source. Saturation is also important for achieving maximum possible operating speeds.[21] This measurement was repeated on the same device with varying top-gate voltages V_{tg} ranging between 0 and 6 V (the maximum value is limited by the dielectric strength of the oxide and at a HfO_2 thickness of 30 nm oxide breakthrough has been

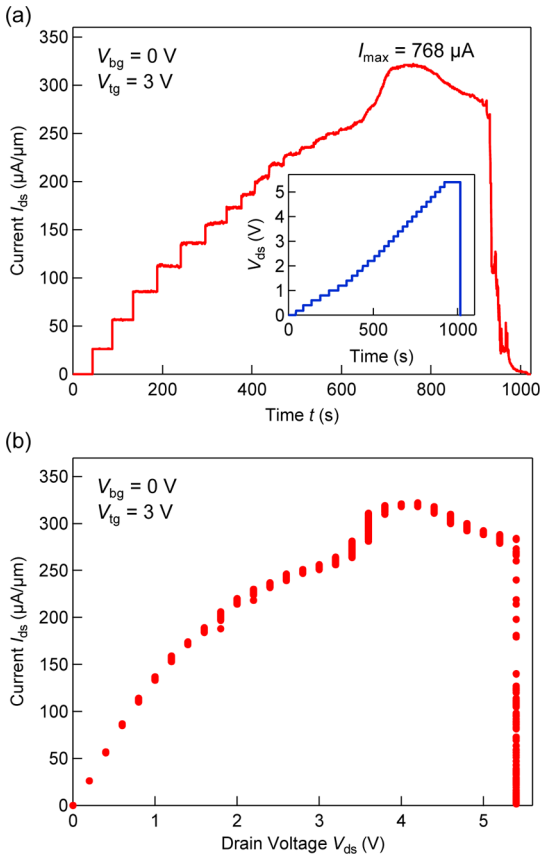

Figure 3. Maximum current density of monolayer MoS_2 FETs. (a) Time trace of the drain current I_{ds} recorded during the breakdown of a monolayer MoS_2 FET. Back-gate voltage V_{bg} = 0 V, top-gate voltage V_{tg} = 3 V. Inset: corresponding V_{ds} *vs* time. V_{ds} is increased in steps of 200 mV approximately every 30 s. The current is allowed to stabilize between the steps. The maximum recorded value of the current for this device is $I_{ds,max}$ = 768 μA (320 μA/μm) for V_{ds} = 4.2 V, which marks the beginning of the electrical deterioration of the device and its current-carrying capacity with final breakdown occurring at V_{ds} = 5.4 V. This corresponds to a current density of $J = 4.9 \times 10^7$ A/cm^2 and represents the highest current density reported for MoS_2 so far. (b) $I_{ds}-V_{ds}$ characteristics for the same measurement as depicted in part a.

observed at V_{tg} values exceeding 8 V). At a top-gate voltage of V_{tg} = 6 V and a drain voltage of V_{ds} = 3 V, the monolayer MoS_2 channel is carrying a current of 344 μA (172 μA/μm). When the thickness of the material (t = 6.5 Å) is taken into account, this corresponds to an exceptionally high current density of more than 2.5×10^7 A/cm^2. For low bias voltages, the curve shows linear and symmetric behavior, indicating that our Au−MoS_2 contacts are ohmic.

The ratio of transconductance to drain conductance ($A = g_m/g_{ds}$) is an important figure of merit, and it represents the highest gain achievable using a single transistor.[20] With relatively high values of transconductance (g_m = 20 μS/μm for V_{ds} = 1 V and g_m = 34 μS/μm for V_{ds} = 4 V) and observed current saturation (g_{ds} < 2 μS/μm), our results show that MoS_2 could be interesting not only for applications in digital electronics[7]

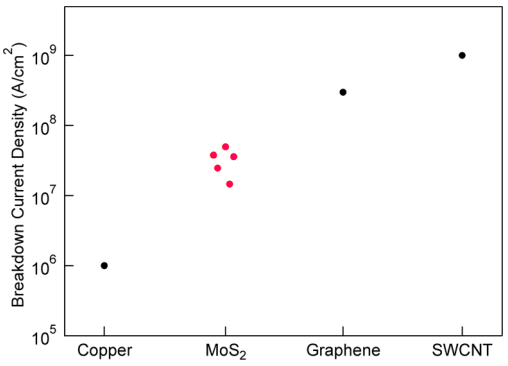

Figure 4. Comparison of breakdown current density for different nanoelectronic materials. The current-carrying capacity of copper is reported to be on the order of 10^6 A/cm^2. Breakdown currents demonstrated in this study for a single layer of semiconducting MoS_2 are close to 5×10^7 A/cm^2. This value is 50 times higher than the electromigration-limited current-carrying capacity of copper.[35] For graphene and metallic single-walled carbon nanotubes, values on the order of 10^8 and 10^9 A/cm^2 for devices on SiO_2 substrates have been reported in the literature.[32,33]

but also for analog applications where it could offer gain >10.

We further investigate the high current-carrying capacity and electrical breakdown of monolayer MoS_2 using two different measurement schemes. In the first one, the V_{ds} is increased in steps of 200 mV approximately every 30 s in order to keep the current flowing under constant conditions for a short period of time. This stepwise increase of V_{ds} is continued until the device breaks down. The time dependence of the drain current for a typical device at the back-gate voltage of V_{bg} = 0 V and a top-gate voltage V_{tg} = 3 V is shown in Figure 3a with the corresponding $I_{ds}-V_{ds}$ dependence presented in Figure 3b. For small values of the drain voltage, the drain current increases as a linear function of the voltage, and above ~1 V, the current begins to saturate, reaching a value of 600 μA (250 μA/μm) for V_{ds} = 3.4 V. Further increase in bias voltage results in a rapid increase of the current, possibly due to Joule heating-induced contact annealing, up to a value of 768 μA (320 μA/μm) for V_{ds} = 4.2 V, which is the maximum recorded current for this device. With the thickness of a monolayer of t = 6.5 Å, this corresponds to a current density of 4.9×10^7 A/cm^2. Further increase of the voltage results in a gradual current decrease and complete failure at a bias voltage of V_{ds} = 5.4 V. The described behavior has been similarly observed for five additional devices. We have also used a second measurement method in which the drain voltage V_{ds} is continuously swept between increasing values of maximal voltage until breakdown occurs. Both methods result in similar maximal current values.

We compare the breakdown current density of monolayer MoS_2 with other typical nanoelectronic materials in Figure 4. Record values for maximum current densities are reported for graphene on

SiO_2 (>10^8 A/cm^2),[32] metallic single-walled carbon nanotubes (>10^9 A/cm^2),[33] and copper (~10^6 A/cm^2).[34] Considering that MoS_2 is a semiconductor, the extracted maximum current density demonstrated is extremely high and is 50 times higher than the limit set for metals by electromigration.[35] This is due to strong intralayer Mo−S covalent bonds[8,36] which are much stronger than metallic bonds. Integration with high thermal conductivity substrates such as diamond[37] could result in further increase of breakdown current density.

CONCLUSION

To summarize, we have produced high-performance 2D transistors based on monolayer MoS_2 showing the highest on-current, highest transconductance and highest estimated mobility reported to date for a 2D transition metal dichalcogenide, while keeping the extremely high room-temperature current on/off ratio of 10^8. Our transistors with a channel length of 500 nm and no underlap show drain current saturation for the first time in monolayer MoS_2, with drain conductance g_{ds} lower than 2 μS and maximum transconductance of $g_m = 34\ \mu S/\mu m$. We also find that monolayer MoS_2 can support large current densities, close to 5×10^7 A/cm^2, exceeding breakdown current density of copper by a factor of 50.

Our results demonstrate that MoS_2 is suitable for the production of high-performance transistors with high internal gain capable of supporting high current densities. This is an important step in realizing 2D nanoelectronic circuits and devices characterized with high-performance, low-power dissipation, and low cost.

METHODS

Single layers of MoS_2 are exfoliated from commercially available crystals of molybdenite (SPI Supplies Brand Moly Disulfide)[28] using the scotch-tape micromechanical cleavage technique method pioneered for the production of graphene. After 90 nm thick Au contact deposition, devices are annealed in 100 sccm of Ar at 200 °C for 2 h.[38] ALD is performed in a commercially available system (Beneq) using a reaction of H_2O with tetrakis(ethyl methylamido)hafnium. Electrical characterization is carried out using an Agilent E5270B parameter analyzer and a home-built shielded probe station with micromanipulated probes.

Conflict of Interest: The authors declare no competing financial interest.

Acknowledgment. The authors thank B. Radisavljevic for advice with device fabrication. Device fabrication was carried out partly in the EPFL Center for Micro/Nanotechnology (CMI). Thanks go to Z. Benes and J. Pernollet (CMI) for technical support with SEM and electron-beam lithography. This work was financially supported by the European Research Council (Grant No. 240076, FLATRONICS) and the Swiss Nanoscience Institute (NCCR Nanoscience).

REFERENCES AND NOTES

1. Novoselov, K. S.; Geim, A. K.; Morozov, S. V.; Jiang, D.; Katsnelson, M. I.; Grigorieva, I. V.; Dubonos, S. V.; Firsov, A. A. Two-Dimensional Gas of Massless Dirac Fermions in Graphene. *Nature* **2005**, *438*, 197–200.
2. Zhang, Y.; Tan, Y.-W.; Stormer, H. L.; Kim, P. Experimental Observation of the Quantum Hall Effect and Berry's Phase in Graphene. *Nature* **2005**, *438*, 201–204.
3. Joensen, P.; Frindt, R. F.; Morrison, S. R. Single-Layer MoS_2. *Mater. Res. Bull.* **1986**, *21*, 457–461.
4. Mak, K. F.; Lee, C.; Hone, J.; Shan, J.; Heinz, T. F. Atomically Thin MoS_2: A New Direct-Gap Semiconductor. *Phys. Rev. Lett.* **2010**, *105*, 136805.
5. Radisavljevic, B.; Radenovic, A.; Brivio, J.; Giacometti, V.; Kis, A. Single-Layer MoS_2 Transistors. *Nat. Nanotechnol.* **2011**, *6*, 147–150.
6. Radisavljevic, B.; Whitwick, M. B.; Kis, A. Small-Signal Amplifier Based on Single-Layer MoS_2. *Appl. Phys. Lett.* **2012**, *101*, 043103.
7. Radisavljevic, B.; Whitwick, M. B.; Kis, A. Integrated Circuits and Logic Operations Based on Single-Layer MoS_2. *ACS Nano* **2011**, *5*, 9934–9938.
8. Bertolazzi, S.; Brivio, J.; Kis, A. Stretching and Breaking of Ultrathin MoS_2. *ACS Nano* **2011**, *5*, 9703–9709.
9. Xiao, D.; Liu, G.-B.; Feng, W.; Xu, X.; Yao, W. Coupled Spin and Valley Physics in Monolayers of MoS_2 and Other Group-VI Dichalcogenides. *Phys. Rev. Lett.* **2012**, *108*, 196802.
10. Mak, K. F.; He, K.; Shan, J.; Heinz, T. F. Control of Valley Polarization in Monolayer MoS_2 by Optical Helicity. *Nat. Nanotechnol.* **2012**, *7*, 494–498.
11. Novoselov, K. S.; Geim, A. K.; Morozov, S. V.; Jiang, D.; Zhang, Y.; Dubonos, S. V.; Grigorieva, I. V.; Firsov, A. A. Electric Field Effect in Atomically Thin Carbon Films. *Science* **2004**, *306*, 666–669.
12. Novoselov, K. S.; Jiang, D.; Schedin, F.; Booth, T. J.; Khotkevich, V. V.; Morozov, S. V.; Geim, A. K. Two-Dimensional Atomic Crystals. *Proc. Natl. Acad. Sci. U.S.A.* **2005**, *102*, 10451–10453.
13. Coleman, J. N.; Lotya, M.; O'Neill, A.; Bergin, S. D.; King, P. J.; Khan, U.; Young, K.; Gaucher, A.; De, S.; Smith, R. J.; *et al.* Two-Dimensional Nanosheets Produced by Liquid Exfoliation of Layered Materials. *Science* **2011**, *331*, 568–571.
14. Liu, K.-K.; Zhang, W.; Lee, Y.-H.; Lin, Y.-C.; Chang, M.-T.; Su, C.-Y.; Chang, C.-S.; Li, H.; Shi, Y.; Zhang, H.; *et al.* Growth of Large-Area and Highly Crystalline Mos_2 Thin Layers on Insulating Substrates. *Nano Lett.* **2012**, *12*, 1538–1544.
15. Zhan, Y.; Liu, Z.; Najmaei, S.; Ajayan, P. M.; Lou, J. Large-Area Vapor-Phase Growth and Characterization of MoS_2 Atomic Layers on a SiO_2 Substrate. *Small* **2012**, *8*, 966–971.
16. Kam, K. K.; Parkinson, B. A. Detailed Photocurrent Spectroscopy of the Semiconducting Group VIB Transition Metal Dichalcogenides. *J. Phys. Chem.* **1982**, *86*, 463–467.
17. Lebegue, S.; Eriksson, O. Electronic Structure of Two-Dimensional Crystals from *Ab Initio* Theory. *Phys. Rev. B* **2009**, *79*, 115409.
18. Splendiani, A.; Sun, L.; Zhang, Y.; Li, T.; Kim, J.; Chim, C.-Y.; Galli, G.; Wang, F. Emerging Photoluminescence in Monolayer MoS_2. *Nano Lett.* **2010**, *10*, 1271–1275.
19. Kuc, A.; Zibouche, N.; Heine, T. Influence of Quantum Confinement on the Electronic Structure of the Transition Metal Sulfide TS_2. *Phys. Rev. B* **2011**, *83*, 245213.
20. Horowitz, P.; Hill, W. *The Art of Electronics*; Cambridge University Press: Cambridge, UK, 1989.
21. Schwierz, F. Graphene Transistors. *Nat. Nanotechnol.* **2010**, *5*, 487–496.
22. Meric, I.; Han, M. Y.; Young, A. F.; Ozyilmaz, B.; Kim, P.; Shepard, K. L. Current Saturation in Zero-Bandgap, Top-Gated Graphene Field-Effect Transistors. *Nat. Nanotechnol.* **2008**, *3*, 654–659.

23. Bai, J.; Liao, L.; Zhou, H.; Cheng, R.; Liu, L.; Huang, Y.; Duan, X. Top-Gated Chemical Vapor Deposition Grown Graphene Transistors with Current Saturation. *Nano Lett.* **2011**, *11*, 2555–2559.
24. Lin, Y.-M.; Dimitrakopoulos, C.; Jenkins, K. A.; Farmer, D. B.; Chiu, H.-Y.; Grill, A.; Avouris, P. 100-GHz Transistors from Wafer-Scale Epitaxial Graphene. *Science* **2010**, *327*, 662.
25. Yoon, Y.; Ganapathi, K.; Salahuddin, S. How Good Can Monolayer MoS_2 Transistors Be?. *Nano Lett.* **2011**, *11*, 3768–3773.
26. Liu, L.; Kumar, S. B.; Ouyang, Y.; Guo, J. Performance Limits of Monolayer Transition Metal Dichalcogenide Transistors. *IEEE Electron Device Trans.* **2011**, *58*, 3042–3047.
27. Frindt, R. F. Single Crystals of MoS_2 Several Molecular Layers Thick. *J. Appl. Phys.* **1966**, *37*, 1928–1929.
28. Purchased from SPI supplies, www.2spi.com, catalog number 429 ML-AB. Collected by a professional geologist at Otter Lake deposit in Ontario, Canada. Specifications available at http://www.2spi.com/catalog/molybdenum.shtml.
29. Benameur, M. M.; Radisavljevic, B.; Heron, J.-S.; Sahoo, S.; Berger, H.; Kis, A. Visibility of Dichalcogenide Nanolayers. *Nanotechnology* **2011**, *22*, 125706.
30. Jena, D.; Konar, A. Enhancement of Carrier Mobility in Semiconductor Nanostructures by Dielectric Engineering. *Phys. Rev. Lett.* **2007**, *98*, 136805.
31. *The International Technology Roadmap for Semiconductors*, http://www.itrs.net/Links/2009ITRS/Home2009.htm (Semiconductor Industry Association, 2009).
32. Moser, J.; Barreiro, A.; Bachtold, A. Current-Induced Cleaning of Graphene. *Appl. Phys. Lett.* **2007**, *91*, 163513.
33. Yao, Z.; Kane, C. L.; Dekker, C. High-Field Electrical Transport in Single-Wall Carbon Nanotubes. *Phys. Rev. Lett.* **2000**, *84*, 2941–2944.
34. Robertson, J. Growth of Nanotubes for Electronics. *Mater. Today* **2007**, *10*, 36–43.
35. Christou, A. *Electromigration and Electronic Device Degradation*; Wiley: New York, 1994.
36. Ataca, C.; Şahin, H.; Ciraci, S. Stable, Single-Layer Mx_2 Transition-Metal Oxides and Dichalcogenides in a Honeycomb-like Structure. *J. Phys. Chem. C* **2012**, *116*, 8983–8999.
37. Yu, J.; Liu, G.; Sumant, A. V.; Goyal, V.; Balandin, A. A. Graphene-on-Diamond Devices with Increased Current-Carrying Capacity: Carbon sp^2-on-sp^3 Technology. *Nano Lett.* **2012**, *12*, 1603–1608.
38. Ishigami, M.; Chen, J. H.; Cullen, W. G.; Fuhrer, M. S.; Williams, E. D. Atomic Structure of Graphene on SiO_2. *Nano Lett.* **2007**, *7*, 1643–1648.